Shri Mata Vaishno Devi University

Consolidated Result of M. Tech. (Electronics & Communication Engineering)

1st Year (1st Sem.), 2nd Year (3rd Sem.), Jul-Nov, 2017

Dated: 15/01/2018

S.No.	Entry_No.	STUDENT_NAME	SEM	CGPA	SGPA	Credits Earned	BACKLOG LIST
1	17MMC003	DIWANKSHI SHARMA	1	RW			
2	17MMC014	SHIVANI BHAT	1	RW			
3	17MMC018	UMAYIA MUSHTAQ	1	RW			
4	17MMC016	SYED ZAINAB ALTAF	1	RW			
5	17MMC002	ATUL BANOTRA	1	RW			
6	17MMC005	JAVID AHMAD GANIE	1	RW			
7	17MMC015	SYED TOOBA SHAMIM ANDRABI	1	RW			
8	17MMC004	HUMIRAH MAJEED	1	RW			
9	17MMC007	MANTISHA GUPTA	1	RW			
10	17MMC010	MIR YAVAR HAYAT	1	7.5	7.5	22	Nil
11	17MMC006	JYOTI SWAROOP SHARMA	1	RW			
12	17MMC012	NAJA MU SAQIB	1	RW			
13	17MMC001	AABID RASHID WANI	1	RW			
14	17MMC017	TUFAIL AHMAD LONE	1	7.05	7.05	22	Nil
15	17MMC013	SHAH ZAHID YOUSUF	1	RW			
16	17MMC009	MEHUL RAJESH	1	RW			
17	17MMC008	MASOOD AHMAD MALIK	1	RW			
18	17MMC011	MOHIT KUMAR	1	RW			
19	16MMC007	DRUVIKA PANDITA	3	8.57	8.38	60	Nil
20	16MMC008	GAURAV SHARMA	3	8.52	9	60	Nil
21	16MMC001	ADITI GUPTA	3	8.4	8.38	60	Nil
22	16MMC009	KAJAL	3	8.18	8.38	60	Nil
23	16MMC017	TARUN BALI	3	8.18	8.48	60	Nil
24	16MMC003	AMIKA PAL SUNDAN	3	8.15	8.24	60	Nil
25	16MMC012	RISHAB AMLA	3	8.15	8.52	60	Nil
26	16MMC011	RAGINI SHARMA	3	RW			
27	16MMC005	ARUNIMA SHARMA	3	7.67	8.1	60	Nil
28	16MMC016	SONALI MAHAJAN	3	7.63	8.1	60	Nil
29	16MMC006	DRISHTI KAKAR	3	7.62	8.24	60	Nil

Prepared By

Checked/Verified By

Sd/-
JA (Exam)

Sd/-
AR (Exam)

Sd/-
Faculty Incharge(Exam)

Shri Mata Vaishno Devi University

Consolidated Result of M. Tech. (Electronics & Communication Engineering)

1st Year (1st Sem.), 2nd Year (3rd Sem.), Jul-Nov, 2017

Dated: 15/01/2018

30	16MMC002	AKSHITA GUPTA	3	7.52	7.95	60	Nil
31	16MMC013	SADAF NADEEM	3	7.48	7.57	60	Nil
32	16MMC014	SAGUN SHARMA	3	7.4	7.86	60	Nil
33	16MMC015	SHRIYA SUNDHAN	3	7.32	7.81	60	Nil
34	16MMC004	AMIT KUMAR	3	6.72	7.57	60	Nil
35	16MMC010	KANAV RISHI	3	6.47	7.29	60	Nil
36	16MMC018	TRIBHUWAN NARAYAN YADAV	3	6.09	5.95	56	* ECL 6051 Microwave Circuit Design(3) * ECP 7084 Embedded Systems Lab(1)

"All efforts have been made to publish this result after checking the entries properly. However, the result can stand revised in case some discrepancy is observed. Please contact Examination Wing for details of backlog."

** RW : Result Withheld due to pending Feedback

Prepared By

Sd/-
JA (Exam)

Checked/Verified By

Sd/-
AR (Exam)

Sd/-
Faculty Incharge(Exam)