

Faculty Development Program

on

Emerging Issues in VLSI Design

7th May 2018 – 11th May 2018

Sponsored by TEQIP-III



Coordinators

Dr. V. K. Sharma & Dr. S. K. Gupta

School of Electronics and Communication Engineering

Shri Mata Vaishno Devi University

Katra-182320 (J&K)

**Contact: +91-1991-285634, Extn. 2241, +91-9906156276,
+91-9532105756**

Email: vijay.sharma@smvdu.ac.in

www.smvdu.ac.in

About Shri Mata Vaishno Devi University, Katra

Shri Mata Vaishno Devi University, commonly referred to as SMVD University or SMVDU, is a state university on 470-acre (190 ha) campus located near Katra, Jammu and Kashmir. It is situated near the shrine of the Mata Vaishno

Devi, after which it is named. The university is fully residential and provides technical education in the field of engineering, science, management, philosophy and other subjects of contemporary importance, with all technical courses recognized by AICTE, CIC and COA. With the focus on higher learning & research, SMVDU has established itself in the league of eminent institutions of learning in the country. It is located at a distance of 45 km from Jammu Airport and 14 km short of the holy town of Katra, the university is situated on a plateau surrounded by mountains on three sides in the foothills of the Trikuta Range where the shrine of Mata Vaishno Devi is located.

About the FDP

Advances in VLSI technology and its trend towards the low leakage high performance applications makes the academicians and industrialists to work in the field of VLSI design. This FDP will give the participants a valuable resource for enhancing their knowledge about the current issues in the VLSI industry.

Resource persons

Resource persons will be from reputed institutions/ industries.

Course contents are (but not limited to)

MOS Basics, Fundamentals of VLSI design, Requirement of device scaling, Importance of low power, Circuit level design, Device level design, Architectural level design, System level design, ASIC design, Reconfigurable VLSI

architecture for various applications, Front-end and back-end design, MEMS/NEMS, Hands on training on EDA tools.

Objective of the FDP

The objective of this FDP is to provide an exposure to the faculty members/research scholars/PG students in the field of “Emerging Issues in VLSI Design” to enhance their knowledge in the domain.

How to apply

Applicants should apply on online Google form in the prescribed format. Last date for application is 30th April 2018. Lodging and boarding for the outstation participants will be provided at SMVDU guesthouse/hostel at free of cost. There are maximum 20 seats for outstation participants. There is ₹ 1000/- (**refundable**) registration fee for the FDP in form of DD in favour of I/c Head Dept/School of Electronics & Communication Engineering payable at Katra. The DD should be send to the provided address and a scan copy to vijay.sharma@smvdu.ac.in. The registration fees may be refunded after the successful completion of the FDP. Link for online registration for FDP is: <https://docs.google.com/forms/d/e/1FAIpQLScVQa-y5byqvluA3P7ZVG8ATL-YULtTLS1bm9dBbAEDfg15sw/viewform>

Important Dates

Last date for receipt of applications: 30th April 2018

Intimation to selected candidates: 4th May 2018